CLAIMS

1. A memory subsystem with symbol sliced command repowering comprising:

a command register in operable communication with a plurality of memory devices via a plurality of command buses;

wherein said plurality of memory devices is arranged into symbol slices and each symbol slice is configured to be part of a single error correction code packet; and

wherein each command bus of said plurality of command buses is configured to interface between said command register and each memory device in a particular symbol slice.

2. The memory subsystem of Claim 1 further including said command register exhibiting sufficient command bus drivers to support each command bus of said plurality of command buses.

3. The memory subsystem of Claim 1 further including a memory controller, said memory controller in operable communication with said command register including a command bus employing an error correction code.

4. The memory subsystem of Claim 1 wherein said error correction code packet is part of an existing error correction code scheme employed for data error correction.

5. The memory subsystem of Claim 1 further including a memory interface device in operable communication with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said command register including a command bus employing an error correction code.

6. The memory subsystem of Claim 1 wherein said plurality of memory devices and said command register comprise a dual in line memory module.

7. The memory subsystem of Claim 1 further including:

a command register in operable communication with a plurality of memory devices; and

a memory controller, said memory controller in operable communication with said command register including a command bus employing another error correction code.

8. The memory subsystem of Claim 7 further including a memory interface device in operable communication with said plurality of dynamic random access memory modules and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said command register including a command bus employing said error correction code.

9. The memory subsystem of Claim 7 wherein said plurality of memory devices and said command register comprise a dual in line memory module.

10. The method of command bus redundancy in a memory subsystem comprising:

configuring a plurality of memory devices into symbol slices, each symbol slice configured to be part of a single error correction code packet;

establishing a plurality of command buses, each command bus configured to interface with each memory device in a particular symbol slice; and

configuring a command register with sufficient command bus drivers to support each command bus of said plurality of command buses.

11. The method of Claim 10 further including communicating a memory controller, with said command register employing a command bus employing said error correction code.

12. The method of Claim 10 wherein said error correction code packet is part of an existing error correction code scheme employed for data error correction.

13. The method of Claim 10 further including communicating a memory interface device with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said register including a command bus employing an error correction code.

14. The method of Claim 10 wherein said plurality of memory devices and said command register comprise a dual in line memory module.

15. The method of Claim 10 further including:

communicating a command register with a plurality of memory devices;

communicating a memory controller with said command register, said communicating including a command bus employing another error correction code.

16. The method of Claim 15 further including communicating a memory interface device with said plurality of memory devices and said memory controller, with at least one of a command bus between said memory controller and said memory interface and a command bus between said memory interface and said register including a command bus employing said error correction code.

17. A system for command bus redundancy in a memory subsystem comprising:

a means for configuring a memory device array into symbol slices, each symbol slice configured to be part of a single error correction code packet;

a means for establishing a plurality of command buses, each command bus configured to interface with each memory device in a particular symbol slice; and

a means for configuring a command register with sufficient command bus drivers to support each command bus of said plurality of command buses.